UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,209	11/16/2001	Eiki Hashimoto	NEKU 19.181	5984

26304 7590 09/02/2003

KATTEN MUCHIN ZAVIS ROSENMAN
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/015,209	Applicant(s) HASHIMOTO, EIKI	
	Examiner A. M. Thompson	Art Unit 2825	

-- The MAILING DATE of this communication appears on th cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,8,11-15,17 and 20* is/are rejected.

7)☒ Claim(s) *2,4,5,7,9,10,16,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This application 10/015,209 has been examined. Claims 1-20 are pending.

Drawings

1. The drawings are objected to because in Figure 4, *Execution* is misspelled. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: In the abstract, line 8, before the second instance of "inspection", change "a" to - -an - -. At page 16, lines 21 and 22, the acronym *CMOS* is incorrect. Additionally, the Acronym "EB" used in the specification (e.g. at page 21, line 16) in undefined.

Appropriate correction is required.

Claim Objections

3. Claims 1-20 are objected to because of the following informalities: Pursuant to claim 1, at line 8, before "inspection" change "a" to - -an- -. Additionally, at lines 13-16, the phrase "said circuit feature. . .of which said logical design should be executed. . . is confusingly worded and requires rephrasing for clarity. Pursuant to claim 13, at lines 3, before "inspection" change "a" to - -an- -; at line 18, delete "in" and insert with in lieu thereof. Pursuant to Claim 15, at line 25, change "in" to - -with- -. Additionally, lines 18-22 requires rephrasing for clarity. Pursuant to claim 16, at lines 5-6, "the number of times" lacks antecedent basis. Appropriate correction is required.

4. Claims 1-20 are objected to: The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Although the claim language of claims 1-20 should merit a rejection under 35 U.S.C. 112, second paragraph, in this application, Examiner has alternatively interpreted the claims to the best extent possible based on the specification and via these claim objections provided Applicants with the opportunity to appropriately revise and clarify the claim language and phraseology.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 1, 3, 6, 8, 11-15, 17 and 20

6. Claims 1, 3, 6, 8, 11-15, 17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakano et al. (Nakano), U.S. Publication 2001/0044667. Nakano teaches a system of manufacturing a semiconductor integrated circuit including a data-managing center, a designing center, and a manufacturing center.

7. Pursuant to claim 1, which recites a semiconductor circuit designing apparatus (Fig. 21) comprising a circuit design executing unit (Fig. 21) executing a logical design

of a semiconductor integrated circuit; and an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed (¶ [0095]), and wherein said circuit design unit generates a target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of which said logical design should be executed, and wherein said circuit design unit obtains a target inspection item of said inspection item corresponding to said target circuit feature information from said inspection item database section, and wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit in reference to said target inspection item (Figs. 21, 23, the designing center).

8. Pursuant to claim 3, further comprising a layout design unit executing said layout design (Fig. 21 illustrates an automatic layout section); wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit (Fig. 21; Fig. 22, Data-Managing Center), and wherein said circuit design unit provides a result of said inspection with said target semiconductor integrated circuit to said layout design unit (Fig. 22).

9. Pursuant to claim 6, wherein said inspection item database belongs to said circuit design unit (Fig. 23).

10. Pursuant to claim 8, wherein said inspection item database section belongs to said layout design unit (Fig. 21).

11. Pursuant to claim 11, wherein said layout design unit includes a plurality of layout design sections, and wherein said inspection item database belongs to a layout design section (Figs. 22, 23).

12. Pursuant to claim 12, further comprising a data center provided to be different from said circuit design unit and said layout design unit, and wherein said inspection item database section belongs to said data center (see Fig. 21-23).

13. Pursuant to claim 13, which recites a semiconductor circuit designing method, comprising (a) providing an inspection item database section in which a circuit feature of a semiconductor integrated circuit in which a logical design should be executed corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed (¶¶ [0092] and [0095]) ;
(b) notifying a circuit designer executing said logical design of said semiconductor integrated circuit of said inspection item corresponding to said semiconductor integrated circuit retrieved from said inspection item database section (¶ [0096]); and (c) executing said logical design by said circuit designer with reference to said notified inspection item (¶ [0096]).

14. Pursuant to claim 14, further comprising providing said semiconductor integrated circuit in which said notified inspection item is passed to a layout designer executing the layout design (¶ [0102]).

15. Pursuant to claim 15, which recites the semiconductor circuit designing method comprising (e) providing a circuit design unit executing a logical design of a semiconductor integrated circuit (Fig. 21); and (f) providing an inspection item database

section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed (Fig. 20; ¶ [0095]) ; and wherein said circuit design unit generates a target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of said semiconductor integrated circuit of which said logical design should be executed (¶ [0095]-[0097], and wherein said circuit design unit obtains a target inspection of said inspection item corresponding to said target feature information from said inspection item database section, and wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit in reference to said target inspection item (Figs. 21, 23, the designing center).

16. Pursuant to claim 17, further comprising (h) providing a layout design unit executing said layout design (Fig. 21, automatic layout section), and wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit of which said layout design is executed (Fig. 21, Designing Center), with regard to said target inspection item, and wherein said circuit design unit provides a result of said inspection with said target semiconductor integrated circuit to said layout design unit.

17. Pursuant to claim 20, wherein said inspection item database section belongs to said circuit design unit (Figs. 22, 23).

Allowable Subject Matter

18. Claims 2 and 16 contain allowable subject matter. A statement providing reasons for the indication of allowable subject matter follows: The prior art does not teach a model development history database in which an ID data of the circuit design

unit corresponds to the number of inspection failures of the inspection item by the circuit design unit.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703) 306-3329.

20. Responses to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Master's Level Patent Examiner